AMENDMENTS TO THE CLAIMS

1. (Previously presented) A method of making semiconductor device packages, comprising:

forming conductive traces in contact with a top surface of a dielectric substrate;

subsequently, forming a layered assembly by attaching a wafer to said dielectric substrate, such that said conductive traces are in electrical communication with semiconductor devices in said wafer;

forming input/output devices in contact with said conductive traces;

testing semiconductor devices in said wafer; and

subsequently, dicing said layered assembly.

2. (Previously presented) The method of claim 1, further comprising the step of connecting said semiconductor devices to said input/output devices.

3. (Original) The method of claim 2, wherein said testing is conducted through said input/output devices.

4. (Original) The method of claim 3, further comprising the step of discarding one or more defective packages.

5. (Previously presented) The method of claim 1, wherein said step of forming said layered assembly includes the step of adhering said wafer to said dielectric substrate.

6. (Previously presented) The method of claim 5, further comprising the step of electrically connecting said semiconductor devices to ball grid arrays on said dielectric substrate.

7. (Previously presented) The method of claim 6, wherein said connecting step comprises the step of locating wire bonds in openings through said dielectric substrate.

8. (Previously presented) The method of claim 6, wherein said connecting step comprises the step of connecting solder bumps on said wafer to circuit traces on said dielectric substrate.

9. (Original) The method of claim 6, wherein said dicing step is performed by a saw.

10. (Original) The method of claim 6, further comprising the step of providing a metal layer in said layered assembly.

11. (Previously presented) A method of making semiconductor device packages, comprising:

providing conductive structures in contact with a top surface of a dielectric substrate;

subsequently, forming a layered assembly by attaching a semiconductor wafer and a stiff metal layer to said dielectric substrate;

placing ball grid arrays in contact with said conductive structures;

electrically connecting semiconductor devices in said semiconductor wafer to said ball grid arrays;

determining whether the wafer contains a defective semiconductor device; and

subsequently, dicing said layered assembly.

12. (Original) The method of claim 11, wherein said forming step comprises the step of adhering said wafer to said metal layer.

13. (Previously presented) The method of claim 11, wherein said connecting step comprises the step of locating wire bonds in openings in said dielectric substrate.

14. (Previously presented) The method of claim 13, further comprising the step of connecting said wire bonds to conductive traces on said dielectric substrate.

15. (Previously presented) The method of claim 11, wherein said connecting step comprises the step of connecting solder bumps on said wafer to conductive traces on said dielectric substrate.

16. (Previously presented) The method of claim 15, further comprising the step of connecting said traces to conductive vias extending through said dielectric substrate.

17. (Original) The method of claim 11, wherein said dicing step is performed by a saw.

18. (Original) The method of claim 11, further comprising the step of testing said semiconductor devices through said ball grid arrays.

19. (Currently Amended) A method of making semiconductor device packages, comprising:

aligning a plurality of semiconductor devices in a semiconductor wafer with respect to openings in a dielectric tape;

subsequently, attaching said semiconductor wafer to said dielectric tape;

~~subsequently,~~ connecting said semiconductor devices in said wafer to ball grid arrays on said dielectric tape; and

simultaneously dicing said wafer and said dielectric tape.

20. (Original) The method of claim 19, wherein said wafer is optically aligned with respect to said dielectric tape.

21. (Original) The method of claim 19, wherein said wafer is magnetically aligned with respect to said dielectric tape.

22. (Original) The method of claim 21, wherein oppositely charged magnetic elements are provided on said wafer and said tape.

23. (Original) The method of claim 21, further comprising the step of locating a magnetic ring in a charged slot.

Claims 24-34 (Canceled).

35. (Previously presented) A method of handling a plurality of semiconductor devices arrayed in a semiconductor wafer, comprising:

adhering said wafer to a flexible substrate;

connecting said semiconductor devices to respective ball grid arrays located on said flexible substrate;

testing said semiconductor devices through said ball grid arrays; and

subsequently, singulating packages from said wafer and said substrate.

36. (Canceled)

37. (Canceled)

38. (Currently Amended) The method of claim [[37]] 41, further comprising the step of segregating defective packages from other packages.

39. (Previously presented) The method of claim 19, further comprising the step of attaching said dielectric tape to said wafer by applying heat or pressure to the assembly.

40. (Previously presented) The method of claim 19, further comprising the step of evacuating gas from said assembly.

41. (New) The method of claim 35, further comprising the step of identifying defective packages.